Appendix 1:

Office Action dated 3/15/00 for parent application ser. no. 09/146,108

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/146,108	09/03/98	DERDERIAN	

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/146,108	DERDERIAN ET AL.	
	Examiner	Art Unit	
	Kurt M Eaton	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *20 October 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5* .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other:

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of 37 CFR 1.71(a)-(c):

> (a) The specification must include a written description of the invention or discovery and of the manner and process of making and using the same, and is required to be in such full, clear, concise, and exact terms as to enable any person skilled in the art or science to which the invention or discovery appertains, or with which it is most nearly connected, to make and use the same.
>
> (b) The specification must set forth the precise invention for which a patent is solicited, in such manner as to distinguish it from other inventions and from what is old. It must describe completely a specific embodiment of the process, machine, manufacture, composition of matter or improvement invented, and must explain the mode of operation or principle whenever applicable. The best mode contemplated by the inventor of carrying out his invention must be set forth.

The specification is objected to under 37 CFR 1.71 because there is no enabling disclosure in the specification to carry out a limitation claimed in claim 11 which states "etching said initial barrier component within said opening". Read in the context of the claim from which it depends, claim 11 states that the initial barrier component is deposited only within the opening. There is no enabling disclosure within the specification that enables one to selectively form an initial barrier component only within an opening and then etch that initial barrier component.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

4. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not contain an enabling disclosure on the limitation found in claim 11 that states "etching said initial barrier component within said opening". Claim 11 depends from claim 9 which states that the initial barrier component is provided only within the opening. The specification thus does not enable one of ordinary skill in the art to deposit an initial barrier layer only within an opening and then to etch the initial barrier layer.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 48 and 71 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 48 recites the limitation "with a portion of said silicon contact containing oxygen" in lines 2 and 3 of claim 48. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 71 recites the limitation "under said capacitor, ..." in lines 1 and 2 of claim 71. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 20-24, 29-33, 36-38, 43-47, 49-53, 55-57, 59-62, 64, and 66-72 are rejected under 35 U.S.C. 102(b) as being anticipated by Sandhu et al. (U.S. Patent No. 5,506,166).

In re claim 20, Sandhu et al. (herein referred to as Sandhu) (U.S. Patent No. 5,506,166), teaches a method of interfacing a silicon contact (65) with a semiconductor device, including: forming a barrier to diffusion from the silicon contact using a first material (75) layered over the silicon contact; and forming a barrier to oxidation (85) of the silicon contact using a selection of the first material and a second material {Figures 2-8, 9B, 10B, 11B, 12B, and 13B; column 5, line 49 – column 6, line 4; column 6, lines 15-34}.

In re claim 21, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of forming a barrier to oxidation further includes providing a layer of ruthenium oxide {column 6, lines 31-34}.

In re claim 22, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of forming a barrier to diffusion further includes, layering over the silicon contact, a selection of Pt, Ir, Os, Pd, Rh, Ru, and oxides thereof; and wherein the step of forming a barrier to oxidation further includes forming a barrier to oxygen using the abovementioned selection {column 5, lines 57-65}.

In re claim 23, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of forming a barrier to diffusion further includes providing a metal nitride layer; and wherein the step of forming

a barrier to oxidation further includes providing a layer made of either a metal or a metal oxide {column 5, lines 49-65; column 6, lines 15-34}.

In re claim 24, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of forming a barrier to diffusion further includes providing a first layer made of either: a nitride of Ti, W, Rh, and Pt-group metals, an oxide of the Pt-group metals, an alloy of the Pt-group metals, or a boride of a transition metal; and wherein the step of forming a barrier to oxidation further includes providing a second layer over the first layer, wherein the second layer is selected from Pt-group metals and an oxide of Pt-group metals {column 5, lines 49-65; column 6, lines 15-34}.

In re claim 29, Sandhu (U.S. Patent No. 5,506,166) shows a damascene process including: forming a first insulation layer (40) over a semiconductor substrate (7); forming a first hole (50 in drawings, 60 in spec.) in the first insulation layer; forming doped polysilicon (65) in the first hole; and forming a silicon barrier (75) over the doped polysilicon {Figures 2-8, 9B, 10B, 11B, 12B, and 13B; column 4, line 1 – column 6, line 4}.

In re claim 30, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of forming doped polysilicon further includes forming doped polysilicon having a low surface within the first hole {Figure 6; column 5, lines 13-24}.

In re claim 31, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of forming doped polysilicon having a low surface within the first hole includes: generally completely filling the first hole with the doped polysilicon; and etching a portion of the doped polysilicon {Figures 5 and 6; column 5, lines 20-23}.

In re claim 32, Sandhu (U.S. Patent No. 5,506,166) further shows a step of forming an oxygen barrier (85) over the silicon barrier {Figure 11B and 12B; column 6, lines 15-34}.

In re claim 33, Sandhu (U.S. Patent No. 5,506,166) further shows a step of forming an electrical contact enhancement layer (67) under the silicon barrier {Figure 8; column 5, lines 25-48}.

In re claim 36, Sandhu (U.S. Patent No. 5,506,166) shows a method of processing a semiconductor device including: providing a silicon interconnect material (65) contacting an electrically conductive first portion (30) of the semiconductor device; and providing an initial barrier component (75) contacting the interconnect material {Figures 5-8 and 9B; column 5, line 13 – column 6, line 4}.

In re claim 37, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of providing an initial barrier component further includes initially protecting the semiconductor device against silicon diffusion {column 5, lines 57-60}.

In re claim 38, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of providing an initial barrier component further includes initially providing a component capable of protecting the semiconductor device against silicon diffusion after further processing {column 5, lines 57-60}.

In re claim 49, Sandhu (U.S. Patent No. 5,506,166) shows a memory cell including: a transistor; a capacitor; a silicon plug (65) extending from the transistor toward the capacitor and physically separate from the capacitor; and a diffusion barrier (75) between the silicon plug and the capacitor {Figure 13B; column 4, line 1 – column 6, line 65}.

In re claim 50, Sandhu (U.S. Patent No. 5,506,166) shows wherein the diffusion barrier is made of a metal nitride {column 5, line 49 – column 6, line 4}.

In re claim 51, Sandhu (U.S. Patent No. 5,506,166) shows wherein the diffusion barrier is made of titanium nitride {column 5, line 49 – column 6, line 4}.

In re claim 52, Sandhu (U.S. Patent No. 5,506,166) further shows an un-nitridized layer of titanium (67) between the diffusion barrier and the silicon plug {Figure 13B; column 5, lines 25-48}.

In re claim 53, Sandhu (U.S. Patent No. 5,506,166) shows wherein the un-nitridized layer of titanium is a silicided layer of titanium { column 5, lines 25-48}.

In re claim 55, Sandhu (U.S. Patent No. 5,506,166) shows an interface between a poly plug (65) and a storage node of a capacitor including: an electrical contact enhancement layer (67) over the poly plug; a silicon barrier (75) over the electrical contact enhancement layer; and an oxidation protection layer (85) over the silicon barrier and contacting the storage node {Figure 13B; column 4, line 1 – column 6, line 65}.

In re claim 56, Sandhu (U.S. Patent No. 5,506,166) shows wherein the electrical contact enhancement layer is a metal silicide layer; the silicon barrier is a metal nitride layer; and the oxidation protection layer is a layer selected from metals, metal oxides, and metal alloys including Pt {column 5, line 25 – column 6, line 34}.

In re claim 57, Sandhu (U.S. Patent No. 5,506,166) shows wherein the electrical contact enhancement layer and the silicon barrier layer contain the same metal {column 5, line 25 – column 6, line 4}.

In re claim 59, Sandhu (U.S. Patent No. 5,506,166) shows a part of a semiconductor circuit including insulation (40) over an electrically conductive surface (55), wherein the insulation defines an opening (50 in drawings, 60 in spec.) and a hole (50 in drawings, 60 in spec.) from the opening to the surface, wherein the part includes: a conductive material (65) filling about half of the hole in the insulation, wherein the conductive material contacts the surface; and a diffusion barrier (75) at least within the hole and over the conductive material {Figure 13B; column 4, line 1 – column 6, line 65}.

In re claim 60, Sandhu (U.S. Patent No. 5,506,166) shows wherein the diffusion barrier lines the opening {Figure 13B}.

In re claim 61, Sandhu (U.S. Patent No. 5,506,166) further shows an oxygen barrier (85) conformal to the diffusion barrier {Figure 13B}.

In re claim 62, Sandhu (U.S. Patent No. 5,506,166) shows a portion of a semiconductor device having an electrically conductive first element (30), an electrically conductive second element (65), and an electrically conductive third element (95) configured to electrically communicate with the first element through the second element, wherein the portion includes: an oxidation barrier (85) contacting the third element; and a silicon diffusion barrier (75) contacting the oxidation barrier and the second element; wherein the oxidation barrier and the silicon diffusion barrier are configures to act as an electrical communication interface between the second element and the third element {Figure 13B; column 4, line 1 – column 6, line 65}.

In re claim 64, Sandhu (U.S. Patent No. 5,506,166) shows wherein the oxidation barrier is made of ruthenium oxide; and the silicon diffusion barrier is also made of ruthenium oxide {column 5, line 48 – column 6, line 34}.

In re claim 66, Sandhu (U.S. Patent No. 5,506,166) shows an interconnect structure including: a doped polysilicon material (65) having a shape defined be an underlying support structure (55) and an adjacent insulative material (40); an electrically conductive material (95) over the doped polysilicon material and the insulative material; and a silicon barrier (75) between the doped polysilicon material and the electrically conductive material {Figure 13B; column 4, line 1 – column 6, line 65}.

In re claim 67, Sandhu (U.S. Patent No. 5,506,166) shows wherein the silicon barrier contacts the doped polysilicon material the electrically conductive material {Figure 13B; column 5, line 13 – column 6, line 4}.

In re claim 68, Sandhu (U.S. Patent No. 5,506,166) further includes an oxidation protection layer (85) contacting and interposed between the silicon barrier and the electrically conductive material {Figure 13B}.

In re claim 69, Sandhu (U.S. Patent No. 5,506,166) further includes an electrical contact enhancement layer (67) contacting and interposed between the silicon barrier and the doped polysilicon material {Figure 13B}.

In re claim 70, Sandhu (U.S. Patent No. 5,506,166) shows an interface for a semiconductor device including a poly plug (65) contacting a substrate (7) and a capacitor plate (95) over the poly plug including: a diffusion barrier (75) under the capacitor plate and over the poly plug, the diffusion barrier selected from a group consisting of: TiN, WN, Rh, RhN, a Pt-group metal, a nitride of the Pt-group metal, an oxide of the Pt-group metal, an alloy of the Pt-group metal, a boride of a transition metal, and combinations of the above materials {Figure 13B; column 5, line 13 – column 6, line 4}.

In re claim 71, Sandhu (U.S. Patent No. 5,506,166) further shows an oxidation barrier (85) under the capacitor plate, over the diffusion barrier, and including a selection of a Pt-group metal and a oxide of the Pt-group metal {Figure 13B; column 6, line 16-34}.

In re claim 72, Sandhu (U.S. Patent No. 5,506,166) further shows an electrical contact enhancement layer (67) under the diffusion barrier and over the poly plug, including a silicide material {Figure 13B; column 5, lines 25-48}.

11. Claims 43-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Summerfelt.

In re claim 43, Summerfelt shows a method of treating a silicon contact, including: depositing a barrier component onto the silicon contact; and nitridizing the barrier component {Figure 9; column 9, lines 18-28}.

In re claim 44, Summerfelt shows wherein the step of depositing the barrier component further includes siliciding the barrier component {column 9, lines 18-28}.

In re claim 45, Summerfelt further includes a step of discretely siliciding the barrier component {column 9, lines 18-28}.

In re claim 46, Summerfelt shows wherein the step of discretely siliciding the barrier component further includes siliciding at least an un-nitridized portion of the barrier component {column 9, lines 18-28}.

In re claim 47, Summerfelt shows wherein the step of discretely siliciding the barrier component further includes reacting the barrier component with silicon in the silicon contact {column 9, lines 18-28}.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 54, 58, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu (U.S. Patent No. 5,506,166).

In re claim 54, Sandhu (U.S. Patent No. 5,506,166) substantially discloses the invention as claimed but fails to show wherein the silicided layer of titanium is generally as thick as the diffusion barrier.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell of Sandhu (U.S. Patent No. 5,506,166) such that the silicided layer of titanium was generally as thick as the diffusion barrier since the discovery of the optimum or workable ranges of a thickness of a layer involves routine skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimension or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical.

In re claim 58, Sandhu (U.S. Patent No. 5,506,166) shows wherein the contact enhancement layer is of a form $TiSi_x$ and the silicon barrier is made of refractory metals or metal nitrides {column 5, lines 25-47}.

Sandhu (U.S. Patent No. 5,506,166) does not show wherein the silicon barrier is made of tungsten nitride.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form silicon barrier out of tungsten nitride since tungsten nitride is a well known material that prevents the diffusion of silicon and the selection of a known material on the basis of its suitability for its intended use involves only routine skill in the art.

In re claim 65, Sandhu (U.S. Patent No. 5,506,166) teaches wherein the oxidation barrier and the silicon barrier may be made out of RuO_2 {column 5, lines 62-65; column 6, lines 32-34}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the oxidation barrier and the silicon barrier out of a continuous layer of RuO_2 instead of two separate layers since it has been held that forming, in one piece, an article which was formerly formed in two pieces and put together involves only routine skill in the art.

14. Claims 1-8, 12, 13-15, 39-42, and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt.

In re claims 1 and 2, Sandhu (U.S. Patent No. 5,506,166) shows, in an analogous art related to storage cell capacitors for use in DRAM memories, in Figures 2-8, 9B, 10B, 11B, 12B, and 13B a method of establishing electrical communication between a first device and a second device in a semiconductor circuit, including: contacting the first device with a first end of an electrically conductive material (65); depositing a refractory metal layer (66) over the electrically conductive layer; reacting the electrically conductive layer and the refractory metal layer together to form a silicide layer (67) over the electrically conductive material; depositing a barrier component (75) in a nitridized form over the silicide layer, thereby forming an electrically conductive layer/silicide layer/nitridized barrier component structure; and contacting the second device with an upper portion of the nitridized barrier component {column 4, line 1 – column 6, line 65}.

Sandhu (U.S. Patent No. 5,506,166) does not show wherein the barrier component is deposited and is subsequently nitridized.

Summerfelt teaches, in an analogous art related to improving the electrical connections to capacitors, that an electrically conductive layer/silicide layer/nitridized barrier component structure,

wherein the electrically conductive layer, the silicide layer, and the nitridized barrier component of Summerfelt are all made out of the same electrically conductive layer, silicide layer, and nitridized barrier component materials of Sandhu (U.S. Patent No. 5,506,166), may be formed by depositing a refractory metal layer over the electrically conductive layer and then nitridizing the refractory metal layer with a standard process such that the electrically conductive layer and a portion of the refractory metal layer are reacted together to form the silicide layer over the electrically conductive material and a portion of the refractory metal layer is also nitridized {column 9, lines 18-28}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrically conductive layer/silicide layer/nitridized barrier component structure of Sandhu (U.S. Patent No. 5,506,166) using the method and materials of Summerfelt since the method of Summerfelt would remove the step of depositing the barrier component in a nitridized form over the silicide layer and create the silicide layer and the nitridized barrier component simultaneously thereby reducing the fabrication steps in the processing sequence and decreasing the amount of time require to process the device.

In re claim 3, Sandhu (U.S. Patent No. 5,506,166) shows in Figure 13B wherein the step of contacting the first device further includes contacting a transistor (22, 21) with doped silicon (65); and wherein the step of contacting the second device further includes contacting a capacitor {column 4, line 1 – column 5, line 19; column 6, lines 15-65}.

In re claim 4, Sandhu (U.S. Patent No. 5,506,166) shows in Figure 13B wherein the step of contacting the second device further includes contacting a capacitor with a doped polysilicon plug {column 5, lines 13-19; column 6, lines 45-56}.

In re claims 5 and 6, Sandhu (U.S. Patent No. 5,506,166) shows in Figures 2-8, 9B, 10B, 11B, 12B, and 13B a method of processing a semiconductor circuit on a substrate (7) covered with an insulating layer (40), wherein the layer defines an opening (50 in drawings, 60 in spec.) over the substrate, and polysilicon (65) contacts a surface (55) of the substrate and a bottom of the opening, wherein the method includes: depositing a refractory metal layer (66) over the polysilicon; reacting the polysilicon and the refractory metal layer together to form a silicide layer (67) over the polysilicon material; and depositing a barrier component (75) in a nitridized form over the silicide layer, thereby forming an polysilicon/silicide layer/nitridized barrier component structure{column 4, line 1 – column 6, line 65}.

Sandhu (U.S. Patent No. 5,506,166) does not show wherein the barrier component is deposited and is subsequently nitridized.

Summerfelt teaches that a polysilicon/silicide layer/nitridized barrier component structure, wherein the silicide layer, and the nitridized barrier component of Summerfelt are all made out of the same silicide layer, and nitridized barrier component materials of Sandhu (U.S. Patent No. 5,506,166), may be formed by depositing a refractory metal layer over polysilicon and then nitridizing the refractory metal layer with a standard process such that the polysilicon and a portion of the refractory metal layer are reacted together to form the silicide layer over the polysilicon material and a portion of the refractory metal layer is also nitridized {column 9, lines 18-28}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the polysilicon/silicide layer/nitridized barrier component structure of Sandhu (U.S. Patent No. 5,506,166) using the method and materials of Summerfelt since the method of Summerfelt would remove the step of depositing the barrier component in a nitridized form over

the silicide layer and create the silicide layer and the nitridized barrier component simultaneously thereby reducing the fabrication steps in the processing sequence and decreasing the amount of time require to process the device.

In re claim 7, Sandhu (U.S. Patent No. 5,506,166) further includes a step of providing an oxidation protection layer (85) within the opening {Figure 11B; column 6, lines 16-36}.

In re claim 8, Sandhu (U.S. Patent No. 5,506,166) further includes a step of recessing the polysilicon {Figures 5 and 6; column 5, lines 13-24}.

In re claims 12 and 13, Sandhu (U.S. Patent No. 5,506,166) shows in Figures 2-8, 9B, 10B, 11B, 12B, and 13B a method of preparing a semiconductor device including a container (50 in drawings, 60 in spec.) defined by at least one insulating layer (40), including: forming a poly plug (65) extending toward the container and having a surface under the container; depositing a refractory metal layer (66) at least between the poly plug and the container; reacting the poly plug and the refractory metal layer together to form a silicide layer (67) over the poly plug material; and depositing a barrier component (75) in a nitridized form over the silicide layer, wherein the barrier component in a nitridized form is next to the container, thereby forming a poly plug/silicide layer/nitridized barrier component structure {column 4, line 1 – column 6, line 65}.

Sandhu (U.S. Patent No. 5,506,166) does not show wherein the barrier component is deposited and is subsequently nitridized.

Summerfelt teaches that a poly plug/silicide layer/nitridized barrier component structure, wherein the silicide layer, and the nitridized barrier component of Summerfelt are all made out of the same silicide layer, and nitridized barrier component materials of Sandhu (U.S. Patent No. 5,506,166), may be formed by depositing a refractory metal layer over polysilicon and then

nitridizing the refractory metal layer with a standard process such that the poly plug and a portion of the refractory metal layer are reacted together to form the silicide layer over the poly plug material and a portion of the refractory metal layer is also nitridized {column 9, lines 18-28}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the poly plug/silicide layer/nitridized barrier component structure of Sandhu (U.S. Patent No. 5,506,166) using the method and materials of Summerfelt since the method of Summerfelt would remove the step of depositing the barrier component in a nitridized form over the silicide layer and create the silicide layer and the nitridized barrier component simultaneously thereby reducing the fabrication steps in the processing sequence and decreasing the amount of time require to process the device.

In re claim 14, Sandhu (U.S. Patent No. 5,506,166) further includes in Figure 11B a step of depositing an oxidation protection layer (85) within the container and over the barrier component in a nitridized form {column 6, lines 15-34}

In re claim 15, Sandhu (U.S. Patent No. 5,506,166) shows in Figure 7 wherein the step of depositing the refractory metal layer further includes lining the container with the refractory metal layer.

In re claim 15, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the refractory metal layer of Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt lining the container would have been nitridized during the nitridizing step of Summerfelt since the nitridizing step of Summerfelt nitridizes the refractory metal layer material.

In re claim 39, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of initially providing the initial barrier component further includes providing a component capable of

protecting the semiconductor device against silicon diffusion during subsequent high temperature anneals{column 5, lines 49-60}.

Sandhu (U.S. Patent No. 5,506,166) does not show forming the initial barrier component by nitridizing it.

Summerfelt teaches that an initial barrier component may be formed by depositing a refractory metal layer over a silicon interconnect material and then nitridizing the refractory metal layer whereby a conductivity enhancement layer is formed at the interface of the silicon interconnect material and the refractory metal layer and the initial barrier component is formed over the conductivity enhancement layer {column 9, lines 18-28}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the initial barrier component of Sandhu (U.S. Patent No. 5,506,166) using the method and materials of Summerfelt since the method of Summerfelt would simultaneously form the initial barrier component as well as a conductivity enhancement layer thereby enhancing the conductivity of the device and thus the performance of the device. It also would have been obvious that since the initial barrier component of Sandhu (U.S. Patent No. 5,506,166) was capable of protecting the semiconductor device against silicon diffusion after being formed, the initial barrier component of Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt would also be capable of protecting the semiconductor device against silicon diffusion after being nitridized.

In re claim 40, Sandhu (U.S. Patent No. 5,506,166) shows in Figures 2-8, 9B, 10B, 11B, 12B, and 13B a method of preventing at least some diffusion from a conductive material (65) in a semiconductor device, including: surrounding a side of the conductive material with an insulator (40); depositing a refractory metal layer (66) onto the conductive material; reacting the conductive

material and the refractory metal layer together to form a silicide layer (67) over the conductive material; and depositing a nitridized barrier component (75) over the silicide layer, thereby forming a conductive material/silicide layer/nitridized barrier component structure {column 4, line 1 – column 6, line 65}.

Sandhu (U.S. Patent No. 5,506,166) does not show wherein the barrier component is deposited and is subsequently nitridized.

Summerfelt teaches that a conductive material/silicide layer/nitridized barrier component structure, wherein the conductive material, the silicide layer, and the nitridized barrier component of Summerfelt are all made out of the same conductive material, silicide layer, and nitridized barrier component materials of Sandhu (U.S. Patent No. 5,506,166), may be formed by depositing a refractory metal layer over the conductive material and then nitridizing the refractory metal layer with a standard process such that the conductive material and a portion of the refractory metal layer are reacted together to form the silicide layer over the conductive material and a portion of the refractory metal layer is also nitridized {column 9, lines 18-28}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the conductive material/silicide layer/nitridized barrier component structure of Sandhu (U.S. Patent No. 5,506,166) using the method and materials of Summerfelt since the method of Summerfelt would remove the step of depositing the barrier component in a nitridized form over the silicide layer and create the silicide layer and the nitridized barrier component simultaneously thereby reducing the fabrication steps in the processing sequence and decreasing the amount of time require to process the device.

In re claim 41, Sandhu (U.S. Patent No. 5,506,166) shows wherein the step of depositing the refractory metal layer further includes depositing the nitridized barrier component onto the conductive material and onto the insulator {Figure 9B}.

In re claim 42, Sandhu (U.S. Patent No. 5,506,166) further includes a step of removing the nitridized barrier component from the insulator {Figure 10B; column 5, line 49 – column 6, line 15}.

In re claim 63, Sandhu (U.S. Patent No. 5,506,166) substantially discloses the invention as claimed but fails to show wherein the oxidation barrier and the silicon diffusion barrier define a continuous iridium layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the silicon diffusion barrier and the oxidation barrier out of iridium since iridium material is a known material may provide a barrier to oxygen and silicon diffusion and the selection of a known material on the basis of its suitability for its intended use involves only routine skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed material or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen materials or upon another variable recited in a claim, the applicant must show that the chosen materials are critical. It also would have been obvious to form the diffusion barriers to oxygen and silicon as a continuous layer since a single layer of material would take less time to deposit than 2 layers, this would thus decrease the amount of time required to fabricate the device.

15. Claims 9, 10, and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt as applied to claims 1-13 above, and further in view of Sandhu et al. (U.S. Patent No. 5,173,327).

In re claim 9, Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt substantially discloses the invention as claimed but fails to show wherein the step of providing refractory metal layer further includes providing the initial barrier component only on the polysilicon.

Sandhu et al. (herein referred to as Sandhu) (U.S. Patent No. 5,173,327) shows, in an analogous art related to semiconductor circuit fabrication, teaches that a refractory metal layer may be selectively deposited onto a polysilicon surface {column 3, line 13 – column 4, line 13}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the refractory metal layer of Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt using the method and materials of Sandhu (U.S. Patent No. 5,173,327) since the method and materials of Sandhu (U.S. Patent No. 5,173,327) would allow the poly plug/silicide layer/nitridized barrier component structure in the container without the need to remove portions of the nitridized barrier component not lying within the container, thereby allowing the device to be processed more quickly.

In re claim 10, Sandhu (U.S. Patent No. 5,173,327) shows wherein the step of providing the refractory metal layer includes depositing the refractory metal layer through selective CVD {column 3, line 13 – column 4, line 13}.

In re claims 16 and 18 Sandhu (U.S. Patent No. 5,506,166) shows in Figures 2-8, 9B, 10B, 11B, 12B, and 13B a method of forming an interface between a transistor (22/21) and a capacitor, wherein the transistor includes a doped portion of a substrate (30), and an in-process poly plug (65) is supported by the doped portion and extends upward along a length to a capacitor site, and wherein the method includes: reducing the poly plug to generally half of the length; depositing a refractory metal layer (66) onto the poly plug, wherein the refractory metal layer has a bottom next

to the poly plug and a top opposite from the bottom; reacting the poly plug and the refractory metal layer together to form a silicide layer (67) over the poly plug material; and depositing a barrier component (75) over the silicide layer, thereby forming a poly plug/silicide layer/nitridized barrier component structure {column 4, line 1 – column 6, line 65}.

Sandhu (U.S. Patent No. 5,506,166) does not show wherein the barrier component is deposited and is subsequently nitridized or wherein the refractory metal layer is selectively CVD layered onto the poly plug.

Summerfelt teaches that a poly plug/silicide layer/nitridized barrier component structure, wherein the poly plug, the silicide layer, and the nitridized barrier component of Summerfelt are all made out of the same poly plug, silicide layer, and nitridized barrier component materials of Sandhu (U.S. Patent No. 5,506,166), may be formed by depositing a refractory metal layer over the poly plug and then nitridizing the refractory metal layer with a standard process such that the poly plug and a portion of the refractory metal layer are reacted together to form the silicide layer over the poly plug material and a portion of the refractory metal layer is also nitridized {column 9, lines 18-28}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the poly plug/silicide layer/nitridized barrier component structure of Sandhu (U.S. Patent No. 5,506,166) using the method and materials of Summerfelt since the method of Summerfelt would remove the step of depositing the barrier component in a nitridized form over the silicide layer and create the silicide layer and the nitridized barrier component simultaneously thereby reducing the fabrication steps in the processing sequence and decreasing the amount of time require to process the device.

Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt does not show wherein the refractory metal layer is selectively CVD layered onto the poly plug.

Sandhu (U.S. Patent No. 5,173,327) shows, in an analogous art related to semiconductor circuit fabrication, teaches that a refractory metal layer may be selectively deposited onto a polysilicon surface {column 3, line 13 – column 4, line 13}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the refractory metal layer of Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt using the method and materials of Sandhu (U.S. Patent No. 5,173,327) since the method and materials of Sandhu (U.S. Patent No. 5,173,327) would allow the poly plug/silicide layer/nitridized barrier component structure in the container without the need to remove portions of the nitridized barrier component not lying within the container, thereby allowing the device to be processed more quickly.

In re claims 17 and 19, Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt and Sandhu (U.S. Patent No. 5,173,327) substantially discloses the invention as claimed but fails to show wherein the step of nitridizing further includes nitridizing generally half of the refractory metal layer or wherein the step of siliciding further includes siliciding generally half of the refractory metal layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to nitridize and silicide generally half of the refractory metal layer of Sandhu (U.S. Patent No. 5,506,166) in view of Summerfelt and Sandhu (U.S. Patent No. 5,173,327) since the discovery of the optimum or workable ranges involves only routine skill in the art and, furthermore, the specification contains no disclosure of either the critical nature of the claimed dimension or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimension

or upon another variable recited in a claim, the applicant must show that the chosen materials are critical.

16. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Summerfelt.

In re claims 25 and 26, Summerfelt shows in Figure 9 a substrate (30) covered with an insulating layer (32); a hole through the insulating layer to the substrate; depositing polysilicon within the hole; depositing at least one metal layer within the hole over the polysilicon, wherein the step of depositing the at least one metal layer includes depositing a titanium layer; siliciding the at least one metal layer, wherein the step of siliciding the at least one metal layer includes siliciding the titanium layer; nitridizing the at least one metal layer, wherein the step of nitridizing the at least one metal layer includes nitridizing the titanium layer; and forming a semiconductor device over the at least one metal layer {column 9, lines 18-28}.

Summerfelt does not show etching the hole through the insulating layer to the substrate; partially plugging the hole with polysilicon; or providing the polysilicon as doped polysilicon.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that since the hole is filled with the nitride/silicide/polysilicon material (50) the polysilicon material could only partially fill (and thus partially plug) the hole. It also would have been obvious to form the hole in the insulating layer by etching since etching insulating material is a well known method by which to form holes in insulating materials and the selection of the etching method to etch holes in insulating materials would have required only routine skill in the art. It also would have been obvious to provide the polysilicon in the hole as doped polysilicon since the selection of a known material on the basis of its suitability for its intended use involves only routine skill in the art.

Furthermore, the specification contains no disclosure of either the critical nature of the claimed material or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen materials or upon another variable recited in a claim, the applicant must show that the chosen materials are critical.

17. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Summerfelt as applied to claim 25 above, and further in view of Sandhu (U.S. Patent No. 5,506,166).

In re claim 27, Summerfelt substantially discloses the invention as claimed but fails to show wherein the step of nitridizing the at least one metal layer includes nitridizing a non-titanium layer.

Sandhu (U.S. Patent No. 5,506,166), in Figure 13B, teaches an equivalent layer to the nitridized at least one metal layer of Summerfelt may be formed by depositing a nitridized non-titanium layer over a previously formed silicided titanium layer {column 5, lines 25-65}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a non-titanium layer over the titanium layer of Summerfelt as in Sandhu (U.S. Patent No. 5,506,166) since the selection of a known material on the basis of its suitability for its intended use as a barrier layer involves only routine skill in the art and the equivalence of depositing a non-titanium layer over a titanium layer prior to nitridizing and siliciding and depositing a titanium layer prior to nitridizing and siliciding for their use in the silicide/nitridized barrier layer metallization and the selection of any of these known equivalents to form a nitridized barrier layer material over a silicided titanium layer would be within the level of ordinary skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed use of a material or any unexpected results arising therefrom. Where patentability is said to be based

upon particular chosen materials and their uses or upon another variable recited in a claim, the applicant must show that the chosen variables are critical.

18. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Summerfelt in view of Sandhu (U.S. Patent No. 5,506,166) as applied to claim 27 above, and further in view of Mathews.

In re claim 28, Summerfelt in view of Sandhu (U.S. Patent No. 5,506,166) substantially discloses the invention as claimed but fails to show wherein the non-titanium layer includes tungsten.

Mathews teaches, in an analogous art related to the formation of refractory metal nitrides suitable for use as diffusion barriers in integrated circuits, that a refractory metal nitride may be formed by first depositing a refractory metal and then nitridizing it in a nitrogen containing ambient {column 4, line 42 – column 5, line 25}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the non-titanium layer of Summerfelt in view of Sandhu (U.S. Patent No. 5,506,166) out of tungsten as in Mathews since tungsten nitride is a well known barrier layer and the selection of a known material on the basis of its suitability for its intended use involves only routine skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed material or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen material or upon another variable recited in a claim, the applicant must show that the chosen variables are critical.

19. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sandhu (U.S. Patent No. 5,506,166) as applied to claim 33 above, and further in view of applicants admitted prior art.

In re claims 34 and 35, Sandhu (U.S. Patent No. 5,506,166) substantially discloses the invention as claimed but fails to show forming a second insulation layer over the first insulation layer; and forming a second hole in the second insulation layer, wherein the second hole is over the first hole.

Applicants admitted prior art shows in Figures 1C and 2 forming a first insulation layer (32) over a semiconductor substrate (50); forming a first hole in the first insulation layer; forming doped polysilicon (28) in the first hole; forming a second insulation layer (30) over the first insulation layer; forming a second hole in the second insulation layer, wherein the second hole is over the first hole; and forming a capacitor within the second hole {page 3, line 20 – page 5, line 10}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a second insulation layer over the first formed insulation layer with a second hole in the second insulation layer over the first hole in the first formed insulation layer of Sandhu (U.S. Patent No. 5,506,166) as in the admitted prior art prior to forming the capacitor structure of Sandhu (U.S. Patent No. 5,506,166) as in the admitted prior art since forming the second hole in the second insulation layer would allow for greater surface area of the capacitor of Sandhu (U.S. Patent No. 5,506,166) to be realized, thus increasing the capacitance of the capacitor and improving the performance of the device.

Conclusion

20. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in

the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.